University of Bahrain
College of Information technology
Department of Computer Engineering

Test (2)

Student Name	
I.D. No.	
Section	

Course Title: Digital Logic
Course number: ITCE 202
Semester: 1
Academic Year: 2008/2009
Duration : 1 hour 15 minutes
Date: 5th January 2009

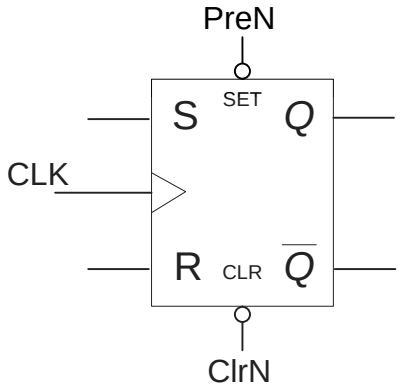
Read the following before you start:
1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

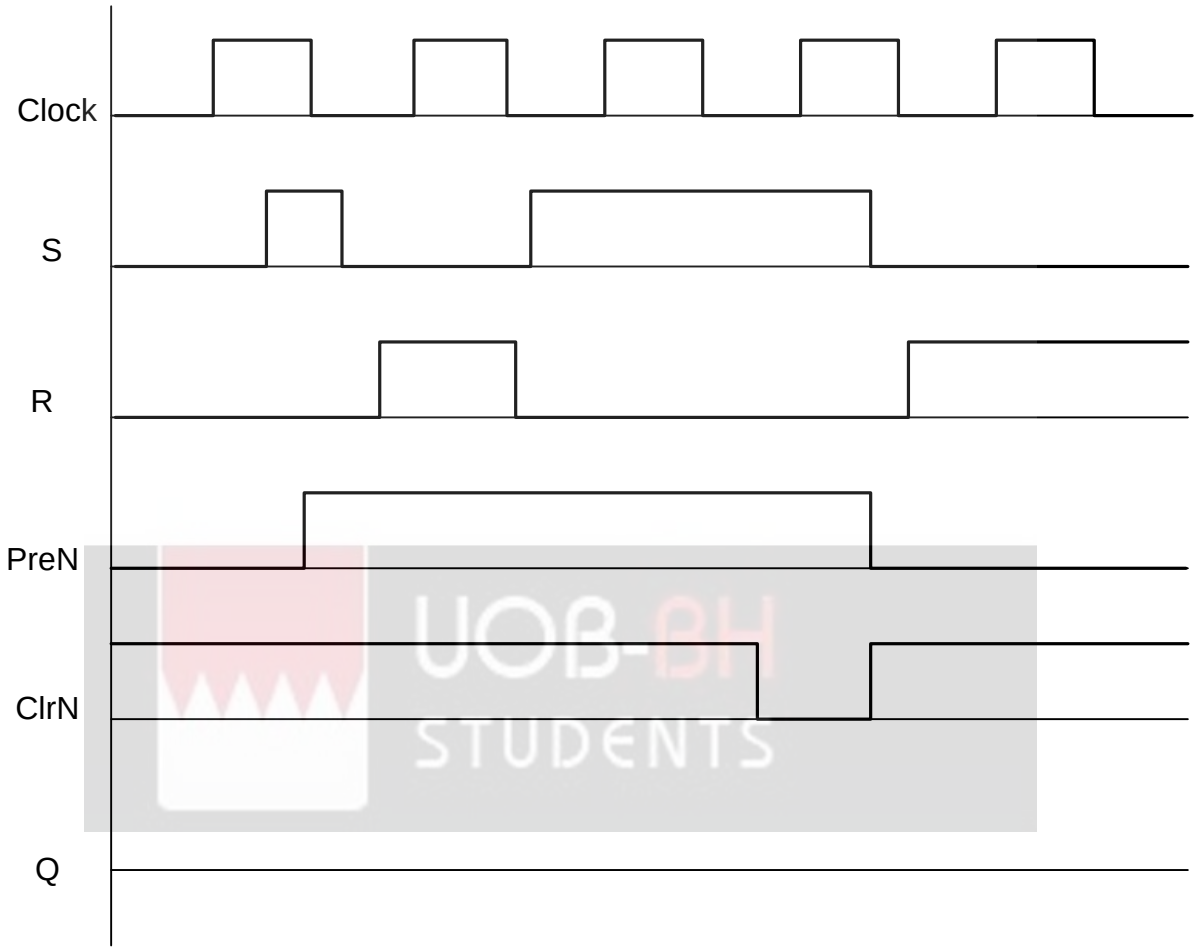
Question	Mark	Mark attained
1	20	
2	15	
3	15	
4	20	
5	30	
Total	100	

Question [1]: [20 mark]

a. Derive the next state equation of an S-R flip flop. [4 marks]

b. Complete the timing diagram of the S-R flip flop shown in the figure. [16 mark]





Question [2] : [15 marks]
Specify the size of a ROM (number of words and number of bits per words) that will accommodate the truth table for the following combinational circuit:
a. A binary multiplier that multiplies 4-bit numbers.

b. A 4-bit adder-subtractor.

c. A BCD-to-seven segment decoder.

Question [3]: [15 marks]
a. Construct the truth table of a ROM to implement the function F= 2 X Y. Where X and Y are 2-bit binary numbers.

b. Draw the internal structure of the ROM showing the first 5 memory lines.

Question [4]: [20 mark]
Design a 3 bit cyclic shift left register using 3 T-flip flop.

Question [5]: [30 mark]

a. Design a 4-bit odd number counter using J-K flip-flops showing all necessary steps required to derive the schematic. [25 mark]

b. Can you improve this design? Justify your answer. Hint: remove any redundant flip flop from your design? [5 marks]